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KLARQUIST SPARKMAN, LLP
16th Floor World Trade Center, 121 S.W. Salmon Street, Portland, Oregon 97204 U.S.A.
PHONE: 503-595-5300 FAX: 503-595-5301

PLEASE DELIVER DIRECTLY TO EXAMINER GUY J. LAMARRE

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Message: Transmitted herewith for filing in the below-identified application is an Examiner Interview Summary. If you do not receive all pages or if you have problems receiving transmittal, please call Justin D. Wagner at (503) 595-5300.

In re application of: Kebichi et al.

Application No. 09/872,212

Filed: May 31, 2001

Confirmation No. 1993

For: SYNCHRONIZATION POINT ACROSS DIFFERENT MEMORY BIST CONTROLLERS

Examiner: Guy J. Lamarre

Art Unit: 2133

Attorney Reference No. 1011-58140-01

CERTIFICATE OF FACSIMILE

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being facsimile transmitted to fax number 703-872-9306 on the date shown below.

Attorney or Agent for Applicant(s) Justin D. Wagner

Date Transmitted July 21, 2005

☒ Examiner Interview Summary (4 pages).

Justin D. Wagner
Registration No. 54,519

July 21, 2005
Date

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PATENT

Attorney Reference Number 1011-58140-01
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Attorney for Applicant

EXAMINER INTERVIEW SUMMARY

Applicants thank Examiner Lamarre for participating in a telephonic interview with the undersigned on July 21, 2005. Claims 1, 13, 19, 30, and 34 were discussed, as were the following references: the example prior art testing environment of FIG. 1 and description ("FIG. 1 Art"), U.S. Patent No. 6,651,202 to Phan ("Phan"), and U.S. Patent No. 6,415,403 to Huang et al. ("Huang").

Applicants asserted the arguments described in detail below.

Agreement was reached that the claims as amended are allowable over the cited art.

I. Allowability of claim 1 over the FIG. 1 Art, Phan, and Huang

Independent claim 1 is directed to a circuit for testing multiple memories and requires: "the resume input comprises a single input pin to the integrated circuit and the signal on the resume input to exit the idle state is asserted through a single channel between automated test equipment (ATE) and the integrated circuit" (emphasis added). For example, FIG. 3 of the present application shows a resume pin 108 that is a single input pin to the integrated circuit (IC) 82 and provides a single channel between ATE 22 and the IC 82.

By contrast, the FIG. 1 Art shows multiple input pins to the IC and thus multiple channels between the ATE and the IC. For example, the present application states at page 3, lines 17-19: "each BIST controller is coupled to a **separate "hold" pin**, such as **hold pins 30, 32**, on the IC

14" and "[t]he hold pins are coupled to the ATE 12, which **controls each hold pin individually**" (emphasis added). This configuration provides several disadvantages, such as the requirement of larger, more expensive ICs to accommodate the multitude of input pins as well as larger, more expensive ATEs to accommodate the multitude of channels.

Phan does not cure the deficiencies of the FIG. 1 Art. For example, Phan is understood to disclose in FIG. 2 an IC and an ATE 160 having **multiple channels in-between** (e.g., FLARESCAN_OUT, FUSE_PROGRAM, FUSESCAN_IN_CLK, and FLARESCAN_IN_CLK). Furthermore, Phan is understood to describe no input resembling a resume input. The inputs described (e.g., signals MEMORY ADDRESS, MEMORY CONTROL, and MEMORY DATA_IN to BIST 102 in FIG. 1) represent inputs other than a resume input, such as memory address bus signals, data bus signals, and control signals.

Huang also does not cure the deficiencies of the FIG. 1 Art. For example, Huang is understood to describe nothing relating to an ATE, much less channels between an ATE and an IC. Furthermore, Huang describes a BIST controller 22 (see FIG. 1) having multiple inputs, but none of the inputs is understood to be anything resembling a resume input. The inputs described in Huang are understood to represent other types of inputs (e.g., state transitions).

The FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single input pin to the integrated circuit and a single channel between automated test equipment (ATE) and the integrated circuit, as required by independent claim 1. Therefore, independent claim 1 and the corresponding dependent claims should be allowable over the cited art.

II. Allowability of claim 13 over the FIG. 1 Art, Phan, and Huang

Independent claim 13 is directed to a circuit for testing multiple memories and requires: "automated test equipment (ATE), wherein the ATE receives the synchronization output through a single channel between the ATE and the integrated circuit" (emphasis added).

As discussed above, the FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single channel between the ATE and the integrated circuit, as required by independent claim 13. Therefore, independent claim 13 and the corresponding dependent claims should be allowable over the cited art.

III. Allowability of claim 19 over the FIG. 1 Art, Phan, and Huang

Independent claim 19 is directed to a method of testing memory and requires: "wherein the synchronization signal is asserted through a single channel to automated test equipment (ATE)" (emphasis added).

As discussed above, the FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single channel to automated test equipment (ATE), as required by independent claim 19. Therefore, independent claim 19 and the corresponding dependent claims should be allowable over the cited art.

IV. Allowability of claim 30 over the FIG. 1 Art, Phan, and Huang

Independent claim 30 is directed to a method of testing memories and requires: "the resume input comprises a single input pin to the integrated circuit and a signal on the resume input is asserted through a single channel between automated test equipment (ATE) and the integrated circuit" (emphasis added).

As discussed above, the FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single input pin to the integrated circuit and a single channel between automated test equipment (ATE) and the integrated circuit, as required by independent claim 30. Therefore, independent claim 30 and the corresponding dependent claims should be allowable over the cited art.

V. Allowability of claim 34 over the FIG. 1 Art, Phan, and Huang

Independent claim 34 is directed to a computer readable medium on which is stored a software tool containing instructions for performing a method that requires: "the resume input comprises a single input pin to an integrated circuit comprising the BIST controller and a signal on the resume input is asserted through a single channel between automated test equipment (ATE) and the integrated circuit" (emphasis added).

As discussed above, the FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single input pin to an integrated circuit and a single channel between automated test equipment (ATE) and the integrated circuit, as required by independent claim 34.

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Therefore, independent claim 34 and the corresponding dependent claims should be allowable over the cited art.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By _____
Justin D. Wagner
Registration No. 54,519

One World Trade Center, Suite 1600
121 S.W. Salmon Street
Portland, Oregon 97204
Telephone: (503) 226-7391
Facsimile: (503) 228-9446